REMARKS

Claims 1 through 84 are currently pending in the application. Claims 43 through 84 are currently under consideration, and Claims 1-42 have been withdrawn in response to a restriction requirement.

This amendment is in response to the Office Action of April 9, 2008.

Information Disclosure Statement(s)

Applicants note the filing of an Information Disclosure Statement herein on April 28, 2008. Applicants respectfully request that the information cited on the PTO/SB/08 be made of record herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Yang et al. (U.S. Patent 6,768,190), in View of Takata et al. (U.S. Patent Publication No. 2002/0027279)

Claims 43, 44, 46, 49 through 53, 55, 64, 65, 68 through 72, and 75 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang et al. (U.S. Patent 6,768,190) in view of Takata et al. (U.S. Patent Publication No. 2002/0027279). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that any combination of the Yang et al. reference in view of the Takata et al. reference does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention of independent claims 43 and 64 of the claimed inventions because any combination of the cited prior art does not teach or suggest the claim limitations of the claimed inventions.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Turning to the cited prior art, the Yang et al. reference teaches or suggests a stack type flip-chip package that utilizes a redistribution circuit on the back of a chip to serve as a bridge for connecting with other chips. The Yang et al. reference does not relate to any conventional semiconductor chip and lead frame mounting arrangement which is encapsulated. The Yang et

al. reference does not teach or suggest the elimination of the substrate therefrom or the inclusion of a die pad or support therein.

The Takata et al. reference teaches or suggests in drawing Fig. 4 and the specification associated therewith electrode pads 17a and 17c located on the upper surface of a semiconductor chip 11 connected through metal wires 14 to the inner leads 13a of a lead frame which extend over and cover a portion of the upper surface of the semiconductor chip 11 as well as the upper surface of the semiconductor chip 11 being protected with a polyimide coating having a thickness of 8.5μm. The inner leads 13a are pressed against the upper surface of the semiconductor chip 11 by a jig during the connection of the metal wires 14 to the electrode pads 17a and 17c. The Takada et al. reference teaches or suggests that by varying the pattern of the electrode pads to vary the thickness of the coating of polyimide on the upper surface of the semiconductor chip 11 the modulus of elasticity of the semiconductor chip 11 may be affected. There in no teaching or suggestion that the electrode pads 17a and 17c either relieve stress or protect the upper surface of the semiconductor chip 11 whatsoever in the Takata et al. reference. In The Takata reference only the thickness of the coating of polyimide on the upper surface of the semiconductor chip 11 varies the stress on the semiconductor chip 11. Further, the Takata et al. reference sets forth in specification paragraph [0055] through [0059] equations for calculating the geometrical moment of inertia for the semiconductor device when it is removed from a mold when a lead frame having a die support as part of the lead frame to limit the bending moment on the encapsulated semiconductor chip by varying the thickness of the encapsulation and the use of a die support. In specification paragraphs [0076] through [0077] a semiconductor chip using a lead frame having no die support is discussed wherein if the ratio of the combination of a semiconductor chip and encapsulation is less than 0.46 no die support is required. Nowhere in the Takata et al. reference is there any discussion of the use of a varying bond pad pattern reducing the bending moment of the combination of a semiconductor chip, lead frame, and encapsulation material when the encapsulated semiconductor chip and lead frame are removed from the mold cavity. At best, the Takata et al. reference teaches or suggests that as the combination of a semiconductor chip, lead frame, and encapsulation material are made thicker, the lower the bending moment on the encapsulated semiconductor chip and lead frame due to the ejection pins removing the encapsulated semiconductor chip and lead frame from the mold while the thinner the

encapsulated semiconductor chip and lead frame the greater the bending moment on the encapsulated semiconductor chip and lead frame by the ejector pins removing the encapsulated semiconductor chip and lead frame from the mold. There is no description, teaching for suggestion whatsoever in the Takata et al. reference as to the variation of the bond pad pattern on the active surface of the semiconductor chip reducing the bending moment on the encapsulated semiconductor chip and lead frame. Solely the ratio of the combination of a semiconductor chip and encapsulation being less than 0.46 determines whether or not a die support is required to reduce to bending moment on the encapsulated semiconductor chip and lead frame.

Applicants assert that any combination of the Yang et al. reference in view of the Takata et al. reference does not teach or suggest the claim limitations of the claimed inventions of independent claims 43 and 64 calling for "forming an area of metal on a surface of the semiconductor die having the size of no greater than a bond pad for a semiconductor die free of connection to a circuit of the semiconductor die or another semiconductor die; and performing one of decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die" and "performing on a semiconductor die having an active surface and an inactive surface, the semiconductor die including at least one bond pad formed on a portion of the active surface connected to the at least one circuit and at least one bond pad having solely the size of a bond pad for a semiconductor die absent connection to a circuit of the semiconductor die or a circuit of another semiconductor die formed on a portion of the inactive surface, lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die for distribution of forces from stress on the semiconductor die by circuits located on the active surface of the semiconductor die".

Applicants assert that neither the Yang et al. reference contains any teaching or suggestion whatsoever regarding such claim limitations in reference to the distribution circuits on the back of the chip nor the Takata et al. reference contains any teaching or suggestion whatsoever regarding electrode pads 17a and 17c in drawing Fig. 4 but only teaches or suggests the use of a die pad or support with a lead frame when the ratio of the combination of a

semiconductor chip, lead frame and encapsulation is less than 0.46, nor any combination of the Yang et al. reference in view of the Takata et al. reference contains any teaching or suggestion as to such claim limitations as to how to modify the redistribution circuit, not a bond pad the size of a bond pad, on the back of the chip in Yang et al. based on any teaching or suggestion regarding electrode pads 17a and 17c on the active surface of the semiconductor chip of the Takata et al. reference.

Applicants assert that neither the Yang et al. reference nor the Takata et al. reference nor any combination of the Yang et al. reference in view of the Takata et al. reference teach or suggest any such claim limitations such as set forth in independent claims 43 and 64 whatsoever. At best, Applicants assert that the Takata et al. reference teaches or suggests that in a leads-over-chip configuration if the encapsulation material thickness is sufficiently thick the section modulus of the semiconductor package after encapsulation of the semiconductor chip and leads of the lead frame may be sufficient to avoid the use of a die pad or support if the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46. Applicants assert that such a teaching or suggestion is not related to the claim limitations of independent claims 43 and 64 whatsoever. Applicants assert that based on any teaching or suggestion the Takata et al. reference does not teach or suggest anything regarding a particular distribution pattern of a group of electrode pads and an increase the section modulus of the semiconductor chip for an encapsulated semiconductor chip and lead frame and has no applicable teaching or suggestion regarding the claim limitations of independent claims 43 and 64 whatsoever. Further, Applicants assert that there has been no showing as to how such relates to any such claim limitations of independent claims 43 and 64, particularly to the claim limitations directed to ". . . decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die". Applicants assert that an increase in the section modulus of an encapsulated semiconductor chip and lead frame only reduces the stiffness of the semiconductor chip, and increases the stress to any load applied to the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that only a decrease in the section modulus of an encapsulated semiconductor

chip and lead frame increases the stiffness of the encapsulated semiconductor chip and lead frame and lowers the bending moment on the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that increasing the section modulus of a semiconductor chip only increases the amount of deflection of the semiconductor chip when subjected to a bending moment type load, does nothing to reduce the stress level of the semiconductor chip, and does nothing to decrease the stress acting on the surface of the semiconductor die by stresses from circuits on the active surface of the semiconductor chip whatsoever. At best, Applicants assert that the Takata et al. reference merely teaches or suggests that by using a coating on the surface of a semiconductor chip with any arrangement of electrode pads thereon and thicker encapsulation surrounding the semiconductor chip and lead frame, when the semiconductor chip is subjected to a bending moment from the ejector pins in the mold, the semiconductor chip deflects less from the bending moment. Applicants assert that there has been no showing whatsoever as to how any stress is reduced from the circuits on the active surface of the semiconductor device by any teaching or suggestion of the Takata et al. reference modifying the Yang et al. reference. Therefore, independent claims 43 and 64 are allowable as well as the dependent claims therefrom.

Applicants assert that absent a reason why one of ordinary skill in the art using "common sense" would seek to combine the teachings or suggestions of the cited prior art to make the claimed combination of the cited prior art to solve a problem as set forth in the claim limitations of the claimed inventions, the proposed combination of the cited prior art does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Takeda Chem Indus., Ltd. V. Alphapharm Pty., Ltd. Fed. Cir., No. 06-1329, 6/28/07. Applicants further assert that a reason to combine or modify the cited prior art which is unrelated to the claimed inventions and does not teach or suggest the claimed invention does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 43 and 64.

Applicant further asserts that to establish a *prima facie* case of obviousness the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Additionally, there must be "a reason that would have prompted a person of ordinary skill

in the relevant field to combine the [prior art] elements" in the manner claimed. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1742, 167 L.Ed.2d 705, 75 USLW 4289, 82 U.S.P.Q.2d 1385 (2007). Finally, to establish a *prima facie* case of obviousness there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Furthermore, the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Applicants assert that no such showings have been met in the rejection of claims 43, 44, 46, 49 through 53, 55, 64, 65, 68 through 72, and 75 based upon any combination of the Yang et al. reference in view of the Takata et al. reference under 35 U.S.C. § 103. Applicants assert that the only showings in the Office Action regarding the claimed invention are based solely upon Applicants disclosure, not the cited prior art because the Yang et al. reference and the Takata et al. reference do not teach or suggest anything regarding the claimed inventions. Applicants assert that such is clearly evident from the cited prior art as their has been no reasons stated as to why the Yang et al. flip-chip style semiconductor devices are to be modified to use the teaching or suggestion of the Takata et al. reference to include a die pad or support if the ratio of the thickness of the encapsulation of the Yang et al. semiconductor devices to the semiconductor devices is greater than 0.46 or how the substrate 110 of the Yang et al. reference can be eliminated if the ratio of the thickness of the encapsulation to the semiconductor device is less than 0.46 Applicants assert that if the Yang et al. reference is modified to either include a die pad or support or to delete the substrate 110, Yang et al. reference is destroyed for its intended purpose. Therefore, Applicants assert that it is improper to attempt to modify the Yang et al. reference based on the Takata et al. reference because they teach away from any combination thereof.

Accordingly Applicants therefore assert that presently amended independent claims 43 and 64 are allowable as the propose combination of the cited prior art is a hindsight reconstruction of the claimed inventions based solely upon Applicants' disclosure which is clearly impermissible under 35 U.S.C. § 103.

Obviousness Rejection Based on Yang et al. (U.S. Patent 6,768,190) and Takata et al. (U.S. Patent Publication No. 2002/0027279), and Further in View of Chu et al. (U.S. Patent Publication No. 2004/0099961)

Claims 47, 48, 62, 63, 66, 67, 83, and 84 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang et al. (U.S. Patent 6,768,190) and Takata et al. (U.S. Patent Publication No. 2002/0027279), as applied to Claims 43 and 64 above, and further in view of Chu et al. (U.S. Patent Publication No. 2004/0099961). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that claims 47, 48, 62, 63, 66, 77, 83, and 84 are allowable as they depend from allowable independent claims 43 are 64 for the reasons set forth hereinabove.

Applicants assert that the Yang et al. reference in view of the Takata et al. reference and further view of the Chu et al. reference fail to establish a *prima faice* case of obviousness under 35 U.S.C. § 103 regarding presently amended independent claims 43 and 64 because of the Takata et al. reference and further view of the Chu et al. reference fail to teach or suggest all the claim limitations of presently amended independent claims 43 and 64 as well as dependent claims 47, 48, 62, 63, 66, 77, 83, and 84 therefrom.

Turning to the cited prior art, the Yang et al. reference teaches or suggests a stack type flip-chip package that utilizes a redistribution circuit, not a bond pad having the size of a bond pad, on the back of a chip to serve as a bridge for connecting with other chips. The Yang et al. reference does not relate to any conventional semiconductor chip and lead frame mounting arrangement which is encapsulated. The Yang et al. reference does not teach or suggest the elimination of the substrate therefrom or the inclusion of a die pad or support therein.

The Takata et al. reference teaches or suggests in drawing Fig. 4 and the specification associated therewith electrode pads 17a and 17c located on the upper surface of a semiconductor chip 11 connected through metal wires 14 to the inner leads 13a of a lead frame which extend

over and cover a portion of the upper surface of the semiconductor chip 11 as well as the upper surface of the semiconductor chip 11 being protected with a polyimide coating having a thickness of 8.5μm. The inner leads 13a are pressed against the upper surface of the semiconductor chip 11 by a jig during the connection of the metal wires 14 to the electrode pads 17a and 17c. The Takada et al. reference teaches or suggests that by varying the pattern of the electrode pads to vary the coating of polyimide on the upper surface of the semiconductor chip 11 the modulus of elasticity of the semiconductor chip 11 may be affected. There in no teaching or suggestion that the electrode pads 17a and 17c either relieve stress or protect the upper surface of the semiconductor chip 11 whatsoever in the Takata et al. reference. Further, the Takata et al. reference sets forth in specification paragraph [0055] through [0059] equations for calculating the geometrical moment of inertia for the semiconductor device when it is removed from a mold when a lead frame having a die support as part of the lead frame to limit the bending moment on the encapsulated semiconductor chip by varying the thickness of the encapsulation and the use of a die support. In specification paragraphs [0076] through [0077] a semiconductor chip using a lead frame having no die support is discussed wherein if the ratio of the combination of a semiconductor chip and encapsulation is less than 0.46 no die support is required. Nowhere in the Takata et al. reference is there any discussion of the use of a varying bond pad pattern reducing the bending moment of the combination of a semiconductor chip, lead frame, and encapsulation material when the encapsulated semiconductor chip and lead frame are removed from the mold cavity. At best, the Takata et al. reference teaches or suggests that as the combination of a semiconductor chip, lead frame, and encapsulation material are made thicker, the lower the bending moment on the encapsulated semiconductor chip and lead frame due to the ejection pins removing the encapsulated semiconductor chip and lead frame from the mold while the thinner the encapsulated semiconductor chip and lead frame the greater the bending moment on the encapsulated semiconductor chip and lead frame by the ejector pins removing the encapsulated semiconductor chip and lead frame from the mold. There is no description, teaching for suggestion whatsoever in the Takata et al. reference as to the variation of the bond pad pattern on the active surface of the semiconductor chip reducing the bending moment on the encapsulated semiconductor chip and lead frame. Solely the ratio of the combination of a semiconductor chip and encapsulation being less than 0.46 determines whether or not a die

support is required to reduce to bending moment on the encapsulated semiconductor chip and lead frame.

The Chu et al. reference teaches or suggests a bond pad having more than one layer of material forming the bond pad.

Applicants assert that any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Chu et al. reference does not teach or suggest the claim limitations of the claimed inventions of independent claims 43 and 64 calling for "forming an area of metal on a surface of the semiconductor die having the size of no greater than a bond pad for a semiconductor die free of connection to a circuit of the semiconductor die or another semiconductor die; and performing one of decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die" and "performing on a semiconductor die having an active surface and an inactive surface, the semiconductor die including at least one bond pad formed on a portion of the active surface connected to the at least one circuit and at least one bond pad having solely the size of a bond pad for a semiconductor die absent connection to a circuit of the semiconductor die or a circuit of another semiconductor die formed on a portion of the inactive surface, lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die for distribution of forces from stress on the semiconductor die by circuits located on the active surface of the semiconductor die".

Applicants assert that neither the Yang et al. reference contains no teaching or suggestion whatsoever regarding such claim limitations in reference to the distribution circuits on the back of the chip nor the Takata et al. reference contains any teaching or suggestion whatsoever regarding electrode pads 17a and 17c in drawing Fig. 4 but only teaches or suggests the use of a die pad or support with a lead frame when the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46, nor any combination of the Yang et al. reference in view of the Takata et al. reference contains any teaching or suggestion as to such claim limitations as to how to modify the redistribution circuit, not a bond pad having the size of a bond pad, on the back of the chip in Yang et al. based on any teaching or suggestion regarding

electrode pads 17a and 17c on the active surface of the semiconductor chip of the Takata et al. reference while any combination of the Yang et al. reference in view of the Takata et al. reference fails to teach or suggest the claim limitations of presently amended independent claims 43 and 64 because neither of the references individually contains any such teachings or suggestions and teach away from any combination thereof.

Applicants assert that neither the Yang et al. reference nor the Takata et al. reference nor the Chu et al. reference nor any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Chu et al. reference teach or suggest any such claim limitations such as set forth in independent claims 43 and 64 whatsoever. At best, Applicants assert that the Takata et al. reference teaches or suggests that in a leads-over-chip configuration if the encapsulation material thickness is sufficiently thick the section modulus of the semiconductor package after encapsulation of the semiconductor chip and leads of the lead frame may be sufficient to avoid the use of a die pad or support if the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46. Applicants assert that such a teaching or suggestion is not related to the claim limitations of independent claims 43 and 64 whatsoever. Applicants assert that based on any teaching or suggestion the Takata et al. reference does not teach or suggest anything regarding a particular distribution pattern of a group of electrode pads and an increase the section modulus of the semiconductor chip for an encapsulated semiconductor chip and lead frame and has no applicable teaching or suggestion regarding the claim limitations of independent claims 43 and 64 whatsoever. Further, Applicants assert that there has been no showing as to how such relates to any such claim limitations of independent claims 43 and 64, particularly to the claim limitations directed to ". . . decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die". Applicants assert that an increase in the section modulus of an encapsulated semiconductor chip and lead frame only reduces the stiffness of the semiconductor chip, and increase the stress to any load applied to the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that only a decrease in the section modulus of an encapsulated semiconductor

chip and lead frame increases the stiffness of the encapsulated semiconductor chip and lead frame and lowers the bending moment on the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that increasing the section modulus of a semiconductor chip only increases the amount of deflection of the semiconductor chip when subjected to a bending moment type load, does nothing to reduce the stress level of the semiconductor chip, and does nothing to decrease the stress acting on the surface of the semiconductor die by stresses from circuits on the active surface of the semiconductor chip whatsoever. At best, Applicants assert that the Takata et al. reference merely teaches or suggests that by using a coating on the surface of a semiconductor chip with any arrangement of electrode pads thereon and thicker encapsulation surrounding the semiconductor chip and lead frame, when the semiconductor chip is subjected to a bending moment from the ejector pins in the mold, the semiconductor chip deflects less from the bending moment. Applicants assert that there has been no showing whatsoever as to how any stress is reduced from the circuits on the active surface of the semiconductor device by any teaching or suggestion of the Takata et al. reference modifying the Yang et al. reference. Further, Applicants assert that the Chu et al. reference does not cure any of the deficiencies of any combination of the Yang et al. in view of the Takata et al. reference. Therefore, independent claims 43 and 64 are allowable as well as the dependent claims therefrom, such as claims 47, 48, 62, 63, 66, 77, 83, and 84.

Applicants assert that absent a reason why one of ordinary skill in the art using "common sense" would seek to combine the teachings or suggestions of the cited prior art to make the claimed combination of the cited prior art to solve a problem as set forth in the claim limitations of the claimed inventions, the proposed combination of the cited prior art does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Takeda Chem Indus., Ltd. V. Alphapharm Pty., Ltd. Fed. Cir., No. 06-1329, 6/28/07. Applicants further assert that a reason to combine or modify the cited prior art which is unrelated to the claimed inventions and does not teach or suggest the claimed invention does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 43 and 64.

Applicants assert that the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge,

or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Applicant asserts that such showings have not been met in the rejection of claims 43, 44, 46, 49 through 53, 55, 64, 65, 68 through 72, and 75 based upon any combination of the Yang et al. reference in view of the Takata et al. reference in further view of the Chu et al. reference under 35 U.S.C. § 103. Applicants assert that the only showings in the Final Rejection regarding the claimed invention are based solely upon Applicants disclosure, not the cited prior art because the Yang et al. reference and the Takata et al. reference and the Chu et al. reference do not teach or suggest anything regarding the claimed inventions. Applicants assert that such is clearly evident from the cited prior art as their has been no reasons stated as to why the Yang et al. flip-chip style semiconductor devices are to be modified to use the teaching or suggestion of the Takata et al. reference to include a die pad or support if the ratio of the thickness of the encapsulation of the Yang et al. semiconductor devices to the semiconductor devices is greater than 0.46 or how the substrate 110 of the Yang et al. reference can be eliminated if the ratio of the thickness of the encapsulation to the semiconductor device is less than 0.46 Applicants assert that if the Yang et al. reference is modified to either include a die pad or support or to delete the substrate 110, Yang et al. reference is destroyed for its intended purpose. Therefore, Applicants assert that it is improper to attempt to modify the Yang et al. reference based on the Takata et al. reference because they teach away from any combination thereof. Further, Applicants assert that the Chu et al. reference does not teach or suggest anything whatsoever related to reducing stress in any fashion regarding any semiconductor device.

Accordingly Applicants therefore assert that presently amended independent claims 43 and 64 are allowable as the propose combination of the cited prior art is a hindsight reconstruction of the claimed inventions based solely upon Applicants' disclosure which is clearly impermissible under 35 U.S.C. § 103.

Obviousness Rejection Based on Yang et al. (U.S. Patent 6,768,190), and Takata et al. (U.S. Patent Publication No. 2002/0027279), and Further in View of Doan (U.S. Patent Publication No. 2005/0167798)

Claims 54, 56, 57, 61, 73, 74, 76, and 78 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang et al. (U.S. Patent 6,768,190), and Takata et al. (U.S. Patent Publication No. 2002/0027279), as applied to Claims 43, 49, 64, 66, and 68 above, and further in view of Doan (U.S. Patent Publication No. 2005/0167798). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that claims 54, 56, 57, 61, 73, 74, 76, and 77 are allowable as they depend from allowable independent claims 43 are 64 for the reasons set forth hereinabove.

Applicants assert that the Yang et al. reference in view of the Takata et al. reference and further view of the Doan reference fail to establish a *prima faice* case of obviousness under 35 U.S.C. § 103 regarding presently amended independent claims 43 and 64 because of the Takata et al. reference and further view of the Chu et al. reference fail to teach or suggest all the claim limitations of presently amended independent claims 43 and 64 as well as dependent claims 47, 48, 62, 63, 66, 77, 83, and 84 therefrom.

Turning to the cited prior art, the Yang et al. reference teaches or suggests a stack type flip-chip package that utilizes a redistribution circuit, not a bond pad having the size of a bond pad, on the back of a chip to serve as a bridge for connecting with other chips. The Yang et al. reference does not relate to any conventional semiconductor chip and lead frame mounting arrangement which is encapsulated. The Yang et al. reference does not teach or suggest the elimination of the substrate therefrom or the inclusion of a die pad or support therein.

The Takata et al. reference teaches or suggests in drawing Fig. 4 and the specification associated therewith electrode pads 17a and 17c located on the upper surface of a semiconductor chip 11 connected through metal wires 14 to the inner leads 13a of a lead frame which extend over and cover a portion of the upper surface of the semiconductor chip 11 as well as the upper surface of the semiconductor chip 11 being protected with a polyimide coating having a thickness of 8.5μm. The inner leads 13a are pressed against the upper surface of the semiconductor chip 11 by a jig during the connection of the metal wires 14 to the electrode pads 17a and 17c. The Takada et al. reference teaches or suggests that by varying the pattern of the electrode pads to

vary the coating of polyimide on the upper surface of the semiconductor chip 11 the modulus of elasticity of the semiconductor chip 11 may be affected. There in no teaching or suggestion that the electrode pads 17a and 17c either relieve stress or protect the upper surface of the semiconductor chip 11 whatsoever in the Takata et al. reference. Further, the Takata et al. reference sets forth in specification paragraph [0055] through [0059] equations for calculating the geometrical moment of inertia for the semiconductor device when it is removed from a mold when a lead frame having a die support as part of the lead frame to limit the bending moment on the encapsulated semiconductor chip by varying the thickness of the encapsulation and the use of a die support. In specification paragraphs [0076] through [0077] a semiconductor chip using a lead frame having no die support is discussed wherein if the ratio of the combination of a semiconductor chip and encapsulation is less than 0.46 no die support is required. Nowhere in the Takata et al. reference is there any discussion of the use of a varying bond pad pattern reducing the bending moment of the combination of a semiconductor chip, lead frame, and encapsulation material when the encapsulated semiconductor chip and lead frame are removed from the mold cavity. At best, the Takata et al. reference teaches or suggests that as the combination of a semiconductor chip, lead frame, and encapsulation material are made thicker, the lower the bending moment on the encapsulated semiconductor chip and lead frame due to the ejection pins removing the encapsulated semiconductor chip and lead frame from the mold while the thinner the encapsulated semiconductor chip and lead frame the greater the bending moment on the encapsulated semiconductor chip and lead frame by the ejector pins removing the encapsulated semiconductor chip and lead frame from the mold. There is no description, teaching for suggestion whatsoever in the Takata et al. reference as to the variation of the bond pad pattern on the active surface of the semiconductor chip reducing the bending moment on the encapsulated semiconductor chip and lead frame. Solely the ratio of the combination of a semiconductor chip and encapsulation being less than 0.46 determines whether or not a die support is required to reduce to bending moment on the encapsulated semiconductor chip and lead frame.

The Doan reference teaches or suggests the use of a conductive filled epoxy for a connector.

Applicants assert that any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Doan reference does not teach or suggest the claim limitations of the claimed inventions of independent claims 43 and 64 calling for "forming an area of metal on a surface of the semiconductor die having the size of no greater than a bond pad for a semiconductor die free of connection to a circuit of the semiconductor die or another semiconductor die; and performing one of decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die" and "performing on a semiconductor die having an active surface and an inactive surface, the semiconductor die including at least one bond pad formed on a portion of the active surface connected to the at least one circuit and at least one bond pad having solely the size of a bond pad for a semiconductor die absent connection to a circuit of the semiconductor die or a circuit of another semiconductor die formed on a portion of the inactive surface, lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die for distribution of forces from stress on the semiconductor die by circuits located on the active surface of the semiconductor die".

Applicants assert that neither the Yang et al. reference contains any teaching or suggestion whatsoever regarding such claim limitations in reference to the distribution circuits on the back of the chip nor the Takata et al. reference contains any teaching or suggestion whatsoever regarding electrode pads 17a and 17c in drawing Fig. 4 but only teaches or suggests the use of a die pad or support with a lead frame when the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46, nor any combination of the Yang et al. reference in view of the Takata et al. reference contains any teaching or suggestion as to such claim limitations as to how to modify the redistribution circuit on the back of the chip in Yang et al. based on any teaching or suggestion regarding electrode pads 17a and 17c on the active surface of the semiconductor chip of the Takata et al. reference while any combination of the Yang et al. reference in view of the Takata et al. reference fails to teach or suggest the claim

limitations of presently amended independent claims 43 and 64 because neither of the references individually contains any such teachings or suggestions and teach away from any combination thereof.

Applicants assert that neither the Yang et al. reference nor the Takata et al. reference nor the Doan reference nor any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Doan reference teach or suggest any such claim limitations such as set forth in independent claims 43 and 64 whatsoever. At best, Applicants assert that the Takata et al. reference teaches or suggests that in a leads-over-chip configuration if the encapsulation material thickness is sufficiently thick the section modulus of the semiconductor package after encapsulation of the semiconductor chip and leads of the lead frame may be sufficient to avoid the use of a die pad or support if the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46. Applicants assert that such a teaching or suggestion is not related to the claim limitations of independent claims 43 and 64 whatsoever. Applicants assert that based on any teaching or suggestion the Takata et al. reference does not teach or suggest anything regarding a particular distribution pattern of a group of electrode pads and an increase the section modulus of the semiconductor chip for an encapsulated semiconductor chip and lead frame and has no applicable teaching or suggestion regarding the claim limitations of independent claims 43 and 64 whatsoever. Further, Applicants assert that there has been no showing as to how such relates to any such claim limitations of independent claims 43 and 64, particularly to the claim limitations directed to ". . . decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die". Applicants assert that an increase in the modulus of elasticity of an encapsulated semiconductor chip and lead frame only reduces the stiffness of the semiconductor chip, and increase the stress to any load applied to the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that only a decrease in the section modulus of an encapsulated semiconductor chip and lead frame increases the stiffness of the encapsulated semiconductor chip and lead frame and lowers the bending moment on the encapsulated semiconductor chip and lead frame

when it is removed from the mold by the ejector pins. Applicants assert that increasing the section modulus of a semiconductor chip only increases the amount of deflection of the semiconductor chip when subjected to a bending moment type load, does nothing to reduce the stress level of the semiconductor chip, and does nothing to decrease the stress acting on the surface of the semiconductor die by stresses from circuits on the active surface of the semiconductor chip whatsoever. At best, Applicants assert that the Takata et al. reference merely teaches or suggests that by using a coating on the surface of a semiconductor chip with any arrangement of electrode pads thereon and thicker encapsulation surrounding the semiconductor chip and lead frame, when the semiconductor chip is subjected to a bending moment from the ejector pins in the mold, the semiconductor chip deflects less from the bending moment. Applicants assert that there has been no showing whatsoever as to how any stress is reduced from the circuits on the active surface of the semiconductor device by any teaching or suggestion of the Takata et al. reference modifying the Yang et al. reference. Further, Applicants assert that the Doan reference does not cure any of the deficiencies of any combination of the Yang et al. in view of the Takata et al. reference. Therefore, independent claims 43 and 64 are allowable as well as the dependent claims therefrom, such as claims 54, 56, 57, 61, 73, 74, 76, and 77.

Applicants assert that absent a reason why one of ordinary skill in the art using "common sense" would seek to combine the teachings or suggestions of the cited prior art to make the claimed combination of the cited prior art to solve a problem as set forth in the claim limitations of the claimed inventions, the proposed combination of the cited prior art does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Takeda Chem Indus., Ltd. V. Alphapharm Pty., Ltd. Fed. Cir., No. 06-1329, 6/28/07. Applicants further assert that a reason to combine or modify the cited prior art which is unrelated to the claimed inventions and does not teach or suggest the claimed invention does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 43 and 64.

Applicants assert that the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367

(Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Applicant asserts that such showings have not been met in the rejection of claims 43, 54, 56, 57, 61, 64, 73, 74, 76, and 77 based upon any combination of the Yang et al. reference in view of the Takata et al. reference in further view of the Doan reference under 35 U.S.C. § 103. Applicants assert that the only showings in the Final Rejection regarding the claimed invention are based solely upon Applicants disclosure, not the cited prior art because the Yang et al. reference and the Takata et al. reference and the Doan reference do not teach or suggest anything regarding the claimed inventions. Applicants assert that such is clearly evident from the cited prior art as their has been no reasons stated as to why the Yang et al. flip-chip style semiconductor devices are to be modified to use the teaching or suggestion of the Takata et al. reference to include a die pad or support if the ratio of the thickness of the encapsulation of the Yang et al. semiconductor devices to the semiconductor devices is greater than 0.46 or how the substrate 110 of the Yang et al. reference can be eliminated if the ratio of the thickness of the encapsulation to the semiconductor device is less than 0.46 Applicants assert that if the Yang et al. reference is modified to either include a die pad or support or to delete the substrate 110, Yang et al. reference is destroyed for its intended purpose. Therefore, Applicants assert that it is improper to attempt to modify the Yang et al. reference based on the Takata et al. reference because they teach away from any combination thereof. Further, Applicants assert that the Doan reference does not teach or suggest anything whatsoever related to reducing stress in any fashion regarding any semiconductor device.

Accordingly Applicants therefore assert that presently amended independent claims 43 and 64 are allowable as the propose combination of the cited prior art is a hindsight reconstruction of the claimed inventions based solely upon Applicants' disclosure which is clearly impermissible under 35 U.S.C. § 103. Therefore, presently amended independent claims 43 and 64 are allowable as well as dependent claims 54, 56, 57, 61, 73, 74, 76, and 77.

Obviousness Rejection Based on Yang et al. (U.S. Patent 6,768,190) and Takata et al. (U.S. Patent Publication No. 2002/0027279), and Further in View of Kuo et al. (U.S. Patent Publication No. 2005/0121804)

Claims 45, 58 through 60, and 79 through 82 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang et al. (U.S. Patent 6,768,190) and Takata et al. (U.S. Patent No. 2002/0027279), as applied to Claims 43 and 64 above, and further in view of Kuo et al. (U.S. Patent Publication No. 2005/0121804). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that claims 45, 58 through 60, and 79 through 82 are allowable as they depend from allowable independent claims 43 are 64 for the reasons set forth hereinabove.

Applicants assert that the Yang et al. reference in view of the Takata et al. reference and further view of the Kuo et al. reference fail to establish a *prima faice* case of obviousness under 35 U.S.C. § 103 regarding presently amended independent claims 43 and 64 because of the Takata et al. reference and further view of the Chu et al. reference fail to teach or suggest all the claim limitations of presently amended independent claims 43 and 64 as well as dependent claims 45, 58 through 60, and 79 through 82 therefrom.

Turning to the cited prior art, the Yang et al. reference teaches or suggests a stack type flip-chip package that utilizes a redistribution circuit, not a bond pad having the size of a bond pad, on the back of a chip to serve as a bridge for connecting with other chips. The Yang et al. reference does not relate to any conventional semiconductor chip and lead frame mounting arrangement which is encapsulated. The Yang et al. reference does not teach or suggest the elimination of the substrate therefrom or the inclusion of a die pad or support therein.

The Takata et al. reference teaches or suggests in drawing Fig. 4 and the specification associated therewith electrode pads 17a and 17c located on the upper surface of a semiconductor chip 11 connected through metal wires 14 to the inner leads 13a of a lead frame which extend over and cover a portion of the upper surface of the semiconductor chip 11 as well as the upper surface of the semiconductor chip 11 being protected with a polyimide coating having a thickness of 8.5μm. The inner leads 13a are pressed against the upper surface of the semiconductor chip 11 by a jig during the connection of the metal wires 14 to the electrode pads 17a and 17c. The Takada et al. reference teaches or suggests that by varying the pattern of the electrode pads to

vary the coating of polyimide on the upper surface of the semiconductor chip 11 the modulus of elasticity of the semiconductor chip 11 may be affected. There in no teaching or suggestion that the electrode pads 17a and 17c either relieve stress or protect the upper surface of the semiconductor chip 11 whatsoever in the Takata et al. reference. Further, the Takata et al. reference sets forth in specification paragraph [0055] through [0059] equations for calculating the geometrical moment of inertia for the semiconductor device when it is removed from a mold when a lead frame having a die support as part of the lead frame to limit the bending moment on the encapsulated semiconductor chip by varying the thickness of the encapsulation and the use of a die support. In specification paragraphs [0076] through [0077] a semiconductor chip using a lead frame having no die support is discussed wherein if the ratio of the combination of a semiconductor chip and encapsulation is less than 0.46 no die support is required. Nowhere in the Takata et al. reference is there any discussion of the use of a varying bond pad pattern reducing the bending moment of the combination of a semiconductor chip, lead frame, and encapsulation material when the encapsulated semiconductor chip and lead frame are removed from the mold cavity. At best, the Takata et al. reference teaches or suggests that as the combination of a semiconductor chip, lead frame, and encapsulation material are made thicker, the lower the bending moment on the encapsulated semiconductor chip and lead frame due to the ejection pins removing the encapsulated semiconductor chip and lead frame from the mold while the thinner the encapsulated semiconductor chip and lead frame the greater the bending moment on the encapsulated semiconductor chip and lead frame by the ejector pins removing the encapsulated semiconductor chip and lead frame from the mold. There is no description, teaching for suggestion whatsoever in the Takata et al. reference as to the variation of the bond pad pattern on the active surface of the semiconductor chip reducing the bending moment on the encapsulated semiconductor chip and lead frame. Solely the ratio of the combination of a semiconductor chip and encapsulation being less than 0.46 determines whether or not a die support is required to reduce to bending moment on the encapsulated semiconductor chip and lead frame.

The Kuo et al. reference teaches or suggests the use of a passivation layer and another passivation layer comprising polymer layer.

Applicants assert that any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Kuo et al. reference does not teach or suggest the claim limitations of the claimed inventions of independent claims 43 and 64 calling for "forming an area of metal on a surface of the semiconductor die having the size of no greater than a bond pad for a semiconductor die free of connection to a circuit of the semiconductor die or another semiconductor die; and performing one of decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die" and "performing on a semiconductor die having an active surface and an inactive surface, the semiconductor die including at least one bond pad formed on a portion of the active surface connected to the at least one circuit and at least one bond pad having solely the size of a bond pad for a semiconductor die absent connection to a circuit of the semiconductor die or a circuit of another semiconductor die formed on a portion of the inactive surface, lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die for distribution of forces from stress on the semiconductor die by circuits located on the active surface of the semiconductor die".

Applicants assert that neither the Yang et al. reference contains any teaching or suggestion whatsoever regarding such claim limitations in reference to the distribution circuits on the back of the chip nor the Takata et al. reference contains any teaching or suggestion whatsoever regarding electrode pads 17a and 17c in drawing Fig. 4 but only teaches or suggests the use of a die pad or support with a lead frame when the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46, nor any combination of the Yang et al. reference in view of the Takata et al. reference contains any teaching or suggestion as to such claim limitations as to how to modify the redistribution circuit on the back of the chip in Yang et al. based on any teaching or suggestion regarding electrode pads 17a and 17c on the active surface of the semiconductor chip of the Takata et al. reference while any combination of the Yang et al. reference in view of the Takata et al. reference fails to teach or suggest the claim

limitations of presently amended independent claims 43 and 64 because neither of the references individually contains any such teachings or suggestions and teach away from any combination thereof.

Applicants assert that neither the Yang et al. reference nor the Takata et al. reference nor the Kuo et al. reference nor any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Kuo et al. reference teach or suggest any such claim limitations such as set forth in independent claims 43 and 64 whatsoever. At best, Applicants assert that the Takata et al. reference teaches or suggests that in a leads-over-chip configuration if the encapsulation material thickness is sufficiently thick the section modulus of the semiconductor package after encapsulation of the semiconductor chip and leads of the lead frame may be sufficient to avoid the use of a die pad or support if the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46. Applicants assert that such a teaching or suggestion is not related to the claim limitations of independent claims 43 and 64 whatsoever. Applicants assert that based on any teaching or suggestion the Takata et al. reference does not teach or suggest anything regarding a particular distribution pattern of a group of electrode pads and an increase the section modulus of the semiconductor chip for an encapsulated semiconductor chip and lead frame and has no applicable teaching or suggestion regarding the claim limitations of independent claims 43 and 64 whatsoever. Further, Applicants assert that there has been no showing as to how such relates to any such claim limitations of independent claims 43 and 64, particularly to the claim limitations directed to ". . . decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die". Applicants assert that an increase in the section modulus of an encapsulated semiconductor chip and lead frame only reduces the stiffness of the semiconductor chip, and increase the stress to any load applied to the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that only a decrease in the modulus of elasticity of an encapsulated semiconductor chip and lead frame increases the stiffness of the encapsulated semiconductor chip and lead frame and lowers the bending moment on the encapsulated semiconductor chip and

lead frame when it is removed from the mold by the ejector pins. Applicants assert that increasing the section modulus of a semiconductor chip only increases the amount of deflection of the semiconductor chip when subjected to a bending moment type load, does nothing to reduce the stress level of the semiconductor chip, and does nothing to decrease the stress acting on the surface of the semiconductor die by stresses from circuits on the active surface of the semiconductor chip whatsoever. At best, Applicants assert that the Takata et al. reference merely teaches or suggests that by using a coating on the surface of a semiconductor chip with any arrangement of electrode pads thereon and thicker encapsulation surrounding the semiconductor chip and lead frame, when the semiconductor chip is subjected to a bending moment from the ejector pins in the mold, the semiconductor chip deflects less from the bending moment. Applicants assert that there has been no showing whatsoever as to how any stress is reduced from the circuits on the active surface of the semiconductor device by any teaching or suggestion of the Takata et al. reference modifying the Yang et al. reference. Further, Applicants assert that the Kuo et al. reference does not cure any of the deficiencies of any combination of the Yang et al. in view of the Takata et al. reference. Therefore, independent claims 43 and 64 are allowable as well as the dependent claims therefrom, such as claims 45, 58 through 60, and 79 through 82.

Applicants assert that absent a reason why one of ordinary skill in the art using "common sense" would seek to combine the teachings or suggestions of the cited prior art to make the claimed combination of the cited prior art to solve a problem as set forth in the claim limitations of the claimed inventions, the proposed combination of the cited prior art does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Takeda Chem Indus., Ltd. V. Alphapharm Pty., Ltd. Fed. Cir., No. 06-1329, 6/28/07. Applicants further assert that a reason to combine or modify the cited prior art which is unrelated to the claimed inventions and does not teach or suggest the claimed invention does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 43 and 64.

Applicants assert that the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367

(Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Applicant asserts that such showings have not been met in the rejection of claims 43, 45, 58 through 60, 64, and 79 through 82 based upon any combination of the Yang et al. reference in view of the Takata et al. reference in further view of the Kuo et al. reference under 35 U.S.C. § 103. Applicants assert that the only showings in the Final Rejection regarding the claimed invention are based solely upon Applicants disclosure, not the cited prior art because the Yang et al. reference and the Takata et al. reference and the Kuo et al. reference do not teach or suggest anything regarding the claimed inventions. Applicants assert that such is clearly evident from the cited prior art as their has been no reasons stated as to why the Yang et al. flip-chip style semiconductor devices are to be modified to use the teaching or suggestion of the Takata et al. reference to include a die pad or support if the ratio of the thickness of the encapsulation of the Yang et al. semiconductor devices to the semiconductor devices is greater than 0.46 or how the substrate 110 of the Yang et al. reference can be eliminated if the ratio of the thickness of the encapsulation to the semiconductor device is less than 0.46 Applicants assert that if the Yang et al. reference is modified to either include a die pad or support or to delete the substrate 110, Yang et al. reference is destroyed for its intended purpose. Therefore, Applicants assert that it is improper to attempt to modify the Yang et al. reference based on the Takata et al. reference because they teach away from any combination thereof. Further, Applicants assert that the Kuo et al. reference does not teach or suggest anything whatsoever related to reducing stress in any fashion regarding any semiconductor device.

Accordingly Applicants therefore assert that presently amended independent claims 43 and 64 are allowable as the propose combination of the cited prior art is a hindsight reconstruction of the claimed inventions based solely upon Applicants' disclosure which is clearly impermissible under 35 U.S.C. § 103. Therefore, presently amended independent claims 43 and 64 are allowable as well as dependent claims 45, 58 through 60, and 79 through 82 therefrom.

Applicants submit that claims 43 through 84 are clearly allowable over the cited prior art. Applicants assert that claims 45, 58 through 60, and 79 through 82 are allowable as they depend from allowable independent claims 43 are 64 for the reasons set forth hereinabove.

Applicants assert that the Yang et al. reference in view of the Takata et al. reference and further view of the Kuo et al. reference fail to establish a *prima faice* case of obviousness under 35 U.S.C. § 103 regarding presently amended independent claims 43 and 64 because of the Takata et al. reference and further view of the Chu et al. reference fail to teach or suggest all the claim limitations of presently amended independent claims 43 and 64 as well as dependent claims 45, 58 through 60, and 79 through 82 therefrom.

Turning to the cited prior art, the Yang et al. reference teaches or suggests a stack type flip-chip package that utilizes a redistribution circuit on the back of a chip to serve as a bridge for connecting with other chips. The Yang et al. reference does not relate to any conventional semiconductor chip and lead frame mounting arrangement which is encapsulated. The Yang et al. reference does not teach or suggest the elimination of the substrate therefrom or the inclusion of a die pad or support therein.

The Takata et al. reference teaches or suggests in drawing Fig. 4 and the specification associated therewith electrode pads 17a and 17c located on the upper surface of a semiconductor chip 11 connected through metal wires 14 to the inner leads 13a of a lead frame which extend over and cover a portion of the upper surface of the semiconductor chip 11 as well as the upper surface of the semiconductor chip 11 being protected with a polyimide coating having a thickness of 8.5μm. The inner leads 13a are pressed against the upper surface of the semiconductor chip 11 by a jig during the connection of the metal wires 14 to the electrode pads 17a and 17c. The Takada et al. reference teaches or suggests that by varying the pattern of the electrode pads to vary the coating of polyimide on the upper surface of the semiconductor chip 11 the modulus of elasticity of the semiconductor chip 11 may be affected. There in no teaching or suggestion that the electrode pads 17a and 17c either relieve stress or protect the upper surface of the semiconductor chip 11 whatsoever in the Takata et al. reference. Further, the Takata et al. reference sets forth in specification paragraph [0055] through [0059] equations for calculating the geometrical moment of inertia for the semiconductor device when it is removed from a mold when a lead frame having a die support as part of the lead frame to limit the bending moment on

the encapsulated semiconductor chip by varying the thickness of the encapsulation and the use of a die support. In specification paragraphs [0076] through [0077] a semiconductor chip using a lead frame having no die support is discussed wherein if the ratio of the combination of a semiconductor chip and encapsulation is less than 0.46 no die support is required. Nowhere in the Takata et al. reference is there any discussion of the use of a varying bond pad pattern reducing the bending moment of the combination of a semiconductor chip, lead frame, and encapsulation material when the encapsulated semiconductor chip and lead frame are removed from the mold cavity. At best, the Takata et al. reference teaches or suggests that as the combination of a semiconductor chip, lead frame, and encapsulation material are made thicker, the lower the bending moment on the encapsulated semiconductor chip and lead frame due to the ejection pins removing the encapsulated semiconductor chip and lead frame from the mold while the thinner the encapsulated semiconductor chip and lead frame the greater the bending moment on the encapsulated semiconductor chip and lead frame by the ejector pins removing the encapsulated semiconductor chip and lead frame from the mold. There is no description, teaching for suggestion whatsoever in the Takata et al. reference as to the variation of the bond pad pattern on the active surface of the semiconductor chip reducing the bending moment on the encapsulated semiconductor chip and lead frame. Solely the ratio of the combination of a semiconductor chip and encapsulation being less than 0.46 determines whether or not a die support is required to reduce to bending moment on the encapsulated semiconductor chip and lead frame.

The Kuo et al. reference teaches or suggests the use of a passivation layer and another passivation layer comprising polymer layer.

Applicants assert that any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Kuo et al. reference does not teach or suggest the claim limitations of the claimed inventions of independent claims 43 and 64 calling for "forming an area of metal on a surface of the semiconductor die free of connection to a circuit of the semiconductor die or another semiconductor die; and performing one of decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the

semiconductor die" and "performing on a semiconductor die having an active surface and an inactive surface, the semiconductor die including at least one bond pad formed on a portion of the active surface connected to the at least one circuit and at least one bond pad formed on a portion of the inactive surface, lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die for distribution of forces from stress on the semiconductor die by circuits located on the active surface of the semiconductor die". Applicants assert that neither the Yang et al. reference contains any teaching or suggestion whatsoever regarding such claim limitations in reference to the distribution circuits on the back of the chip nor the Takata et al. reference contains any teaching or suggestion whatsoever regarding electrode pads 17a and 17c in drawing Fig. 4 but only teaches or suggests the use of a die pad or support with a lead frame when the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46, nor any combination of the Yang et al. reference in view of the Takata et al. reference contains any teaching or suggestion as to such claim limitations as to how to modify the redistribution circuit on the back of the chip in Yang et al. based on any teaching or suggestion regarding electrode pads 17a and 17c on the active surface of the semiconductor chip of the Takata et al. reference while any combination of the Yang et al. reference in view of the Takata et al. reference fails to teach or suggest the claim limitations of presently amended independent claims 43 and 64 because neither of the references individually contains any such teachings or suggestions and teach away from any combination thereof.

Applicants assert that neither the Yang et al. reference nor the Takata et al. reference nor the Kuo et al. reference nor any combination of the Yang et al. reference in view of the Takata et al. reference and in further view of the Kuo et al. reference teach or suggest any such claim limitations such as set forth in independent claims 43 and 64 whatsoever. At best, Applicants assert that the Takata et al. reference teaches or suggests that in a leads-over-chip configuration if the encapsulation material thickness is sufficiently thick the section modulus of the semiconductor package after encapsulation of the semiconductor chip and leads of the lead frame may be sufficient to avoid the use of a die pad or support if the ratio of the combination of a semiconductor chip, lead frame and encapsulation is less than 0.46. Applicants assert that such a teaching or suggestion is not related to the claim limitations of independent claims 43 and 64

whatsoever. Applicants assert that based on any teaching or suggestion the Takata et al. reference does not teach or suggest anything regarding a particular distribution pattern of a group of electrode pads and an increase the section modulus of the semiconductor chip for an encapsulated semiconductor chip and lead frame and has no applicable teaching or suggestion regarding the claim limitations of independent claims 43 and 64 whatsoever. Further, Applicants assert that there has been no showing as to how such relates to any such claim limitations of independent claims 43 and 64, particularly to the claim limitations directed to ". . . decreasing stress acting on the surface of the semiconductor die by placing at least one bond pad on an inactive surface of the semiconductor die causing distribution of forces on at least a portion of the semiconductor die from stress on the semiconductor die from circuits located on the active surface of the semiconductor die". Applicants assert that an increase in the section modulus of an encapsulated semiconductor chip and lead frame only reduces the stiffness of the semiconductor chip, and increase the stress to any load applied to the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that only a decrease in the modulus of elasticity of an encapsulated semiconductor chip and lead frame increases the stiffness of the encapsulated semiconductor chip and lead frame and lowers the bending moment on the encapsulated semiconductor chip and lead frame when it is removed from the mold by the ejector pins. Applicants assert that increasing the section modulus of a semiconductor chip only increases the amount of deflection of the semiconductor chip when subjected to a bending moment type load, does nothing to reduce the stress level of the semiconductor chip, and does nothing to decrease the stress acting on the surface of the semiconductor die by stresses from circuits on the active surface of the semiconductor chip whatsoever. At best, Applicants assert that the Takata et al. reference merely teaches or suggests that by using a coating on the surface of a semiconductor chip with any arrangement of electrode pads thereon and thicker encapsulation surrounding the semiconductor chip and lead frame, when the semiconductor chip is subjected to a bending moment from the ejector pins in the mold, the semiconductor chip deflects less from the bending moment. Applicants assert that there has been no showing whatsoever as to how any stress is reduced from the circuits on the active surface of the semiconductor device by any teaching or suggestion of the Takata et al. reference modifying the Yang et al. reference. Further, Applicants assert that the

Kuo et al. reference does not cure any of the deficiencies of any combination of the Yang et al. in view of the Takata et al. reference. Therefore, independent claims 43 and 64 are allowable as well as the dependent claims therefrom, such as claims 45, 58 through 60, and 79 through 82.

Applicants assert that absent a reason why one of ordinary skill in the art using "common sense" would seek to combine the teachings or suggestions of the cited prior art to make the claimed combination of the cited prior art to solve a problem as set forth in the claim limitations of the claimed inventions, the proposed combination of the cited prior art does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Takeda Chem Indus., Ltd. V. Alphapharm Pty., Ltd. Fed. Cir., No. 06-1329, 6/28/07. Applicants further assert that a reason to combine or modify the cited prior art which is unrelated to the claimed inventions and does not teach or suggest the claimed invention does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 43 and 64.

Applicants assert that the reason that would have prompted the combination and the reasonable expectation of success must be found in the prior art, common knowledge, or the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006); MPEP § 2144. Underlying the obvious determination is the fact that statutorily prohibited hindsight cannot be used. *KSR*, 127 S.Ct. at 1742; *DyStar*, 464 F.3d at 1367.

Applicant asserts that such showings have not been met in the rejection of claims 43, 45, 58 through 60, 64, and 79 through 82 based upon any combination of the Yang et al. reference in view of the Takata et al. reference in further view of the Kuo et al. reference under 35 U.S.C. § 103. Applicants assert that the only showings in the Final Rejection regarding the claimed invention are based solely upon Applicants disclosure, not the cited prior art because the Yang et al. reference and the Takata et al. reference and the Kuo et al. reference do not teach or suggest anything regarding the claimed inventions. Applicants assert that such is clearly evident from the cited prior art as their has been no reasons stated as to why the Yang et al. flip-chip style semiconductor devices are to be modified to use the teaching or suggestion of the Takata et al. reference to include a die pad or support if the ratio of the thickness of the encapsulation of the

Yang et al. semiconductor devices to the semiconductor devices is greater than 0.46 or how the substrate 110 of the Yang et al. reference can be eliminated if the ratio of the thickness of the encapsulation to the semiconductor device is less than 0.46 Applicants assert that if the Yang et al. reference is modified to either include a die pad or support or to delete the substrate 110, Yang et al. reference is destroyed for its intended purpose. Therefore, Applicants assert that it is improper to attempt to modify the Yang et al. reference based on the Takata et al. reference because they teach away from any combination thereof. Further, Applicants assert that the Kuo et al. reference does not teach or suggest anything whatsoever related to reducing stress in any fashion regarding any semiconductor device.

Accordingly Applicants therefore assert that presently amended independent claims 43 and 64 are allowable as the propose combination of the cited prior art is a hindsight reconstruction of the claimed inventions based solely upon Applicants' disclosure which is clearly impermissible under 35 U.S.C. § 103. Therefore, presently amended independent claims 43 and 64 are allowable as well as dependent claims 45, 58 through 60, and 79 through 82 therefrom.

Applicants submit that claims 43 through 84 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 43 through 84 and the case passed for issue.

Respectfully submitted,

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